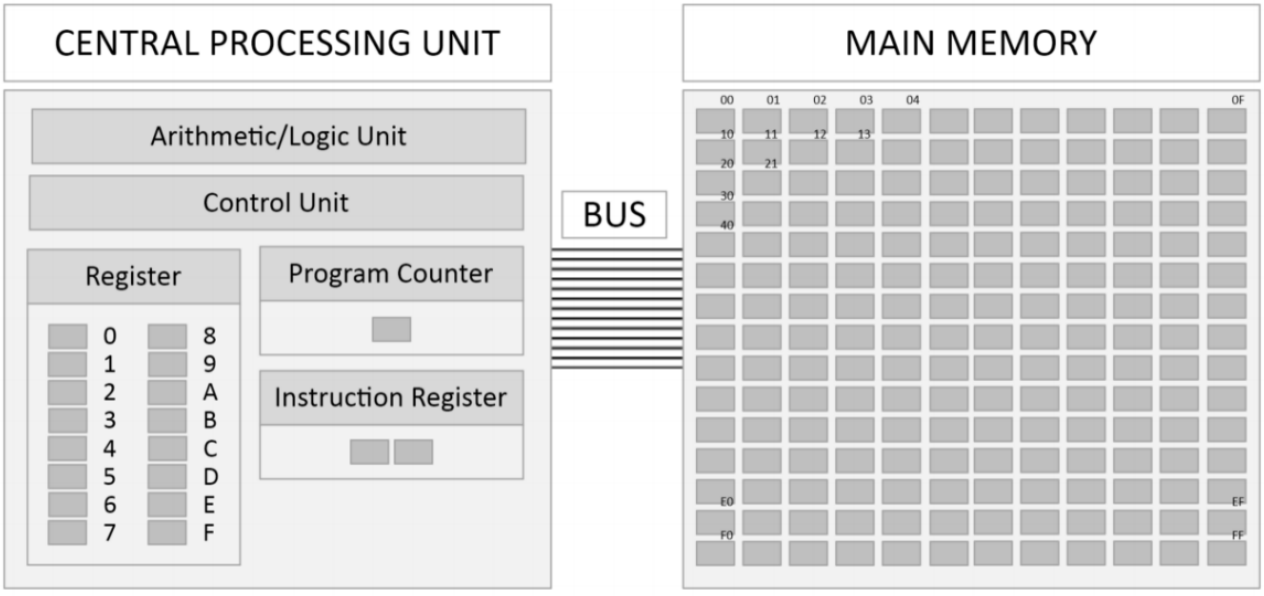
Architecture
of the Example Machine

[Aka VizMachine]

- The machine has 16 general-purpose registers with numbers from 0 to F.
- Each register has a width of one Byte.
- Any distinct register within the instructions is referenced by 4 Bits. (0000 corresponds to register 0, 0100 to register 4, 1111 to register F ...)
- The machine utilizes a Main Memory of 256 Bytes.
- Each memory cell (one Byte) is accessed using an address ranging from 0 to 255(00 to FF hexadecimal).
- Floating-point values are represented as followed: (from most significant bit downwards): 1 Bit prefix (+/-), 3 Bit Exponent, 4 Bit Mantissa.
- Each machine instruction has a length of 2 Byte and consists of an Op-Code with 4 Bit and an operand-field of 12 Bits.
- The following description uses the letters R, S, T within the operand for a hexadecimal number, which points to the number of a register.
- The letters X and Y within the operand point to hexadecimal numbers, which do not represent registers. These represent a hexadecimal value or an address in the memory between 00 and FF.



Op-code	Operand	Description
1	RXY	LOAD register R with data from memory cell with address XY. (Register/Memory Direct Addressing)
2	RXY	LOAD register R with value of (Bit-pattern) XY. (Immediate Value)
3	RXY	STORE data from register R in memory cell with address XY.
4	0RS	MOVE data from register R to register S.
5	RST	ADD data from register S and register T (Two Complement Interpretation), saving the result to register R.
6	RST	ADD data from register S and register T (Floating-Point Interpretation), saving the result to register R.
7	RST	OR of Bit pattern from register S and register T, saving the result to register R.
8	RST	AND of Bit pattern from register S and register T, saving the result to register R.
9	RST	XOR of Bit pattern from register S and register T, saving the result to register R.
A	R0X	ROTATE the Bit pattern in register R one Bit to the right, X-times.
B	RXY	JUMP to instruction in memory cell with the address XY, if the data in register R is equal to the data in register 0.
C	000	HALT.

Additional Operations

Op-code	Operand	Description
D	XYZ	WAIT in milliseconds defined by XYZhex value.
E	RST	WRITE data from register R in memory cell with address given in register T. (Register Indirect)